REMARKS

Summary of the Office Action

Claims 1-31 are pending in the above-identified patent application.

The Examiner has rejected claims 1, 2, 4, 7-10, 12-17, 22, 27, and 30 under 35 U.S.C. § 102(b) as being anticipated by Agrawal et al. U.S. Patent No. 5,740,069 ("Agrawal"). Claims 18-21 and 23-26 have been rejected under 35 U.S.C. § 103(a) as being obvious from Agrawal in view of Schlecher et al. U.S. Patent No. 6,366,120 ("Schlecher").

Each of claims 3, 5, 6, and 11 has been objected to as being dependent upon a rejected base claim, but allowable subject matter has been indicated. Claims 28, 29, and 31 have been allowed.

Summary of Applicants' Reply

Applicants note with appreciation the allowance of claims 28, 29, and 31 and the indication of allowable subject matter in claims 3, 5, 6, and 11. Applicants expressly reserve the right to rewrite any one or more of claims 3, 5, 6, and 11 in independent form if its respective base claim is not ultimately allowed.

Applicants have amended claims 1, 27, and 30 to more particularly define the invention. The Examiner's rejections and objection are respectfully traversed.

Telephonic Interview Summary

On June 28, 2006, a telephonic interview took place between the Examiner and Mr. Chia-Hao La (Reg. No. 57,729). Mr. La wishes to thank the Examiner for the courtesies extended during the telephonic interview.

During the telephonic interview, the Examiner and Mr. La discussed generally the rejection of independent claim 1 in view of Agrawal. The Examiner indicated that claim 1 would be allowable over Agrawal if it were amended to specify that the output bypass did not pass through any multiplexer between the logic elements ("LEs") and the

input/output ("I/O") block. Applicants have amended independent claim 1 accordingly in order to advance prosecution even though applicants maintain that the claim before amendment was allowable over the prior art of record. Applicants have also amended independent claims 27 and 30 to incorporate a similar feature. Detailed arguments in support of applicants' position are presented below.

Applicants' Reply to the
Prior Art Rejections

Claims 1, 2, 4, 7-10, 12-17, 22, 27, and 30 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Agrawal. Claims 18-21 and 23-26 have been rejected under 35 U.S.C. § 103(a) as being obvious from Agrawal in view of Schlecher. The Examiner's rejections are respectfully traversed.

Applicants' invention, as defined by amended independent claim 1, relates to a programmable logic device that includes a plurality of LEs, at least one I/O block, and a signal routing architecture for routing signals among the LEs and the at least one I/O block. The signal routing architecture includes a plurality of horizontal and vertical signal routing conductors, at least one block input multiplexer for selectively providing signals from the routing conductors to the at least one I/O block, and at least one output bypass path for providing a direct connection between an output of an LE and the at least one I/O block, where the at least one output bypass path does not travel through a multiplexer between the plurality of LEs and the at least one I/O block. Independent claim 27 defines a programmable logic device with similar features, and independent claim 30 relates to a method whose features correspond to those of claim 1. The references cited by the Examiner, whether taken singly or in combination, neither show nor suggest the claimed invention.

Applicants' invention, as defined by independent claim 1, includes at least one output bypass path for providing a direct connection between an output from one of

a plurality of LEs and at least one I/O block, where the at least one output bypass path does not pass through a multiplexer between the plurality of LEs and the at least one I/O block. Each of independent claims 27 and 30 includes a feature that corresponds to this feature of claim 1. As discussed in applicants' specification in connection with the illustrative embodiment of FIG. 3A,

> output bypass path 370 is used to directly connect the output of LAB 110 to adjacent I/O block 160. In particular, output bypass path 370 provides a faster connection between the output of LAB 110 and I/O multiplexer 361 than is otherwise possible because the delays associated with a signal traveling through DIM 341 and BIM 351, for example, are avoided.

Applicants' specification, page 16, lines 1-8.

In contrast, Agrawal describes a programmable integrated circuit with configurable logic blocks ("CLBs"), configurable input/output blocks ("IOBs"), and an interconnect network for routing signals between the CLBs and IOBs. The Examiner contends that multiplexer 4501 of FIG. 45 and multiplexer 4603 of FIG. 46 show at least one block input multiplexer for selectively providing signals from signal routing conductors to at least one I/O block, as defined by applicants' independent claim 1. See Office Action, page 3.

As explained by Mr. La during the interview, each of multiplexers 4501 and 4603 resides inside its respective IOB. See Agrawal FIGS. 45 and 46, col. 27, line 50 to col. 31, line 24. As such, they cannot provide signals from routing conductors <u>to</u> at least one I/O block, as defined by applicants' claim 1. Even assuming, for the sake of argument, that each of multiplexers 4501 and 4603 resides outside its respective IOB, Agrawal would still require a signal sent from a CLB to an IOB to pass through a multiplexer between that CLB and that IOB. As discussed by Agrawal in connection with FIG. 53, "[e]ach [IOB] has a

multiplexer receiving a plurality of signals for supply as the output signal to the associated pin. These inputs are shown by the reference O." Col. 35, line 66 to col. 36, line 2. Accordingly, as pointed out by Mr. La during the interview, Agrawal neither shows nor suggests at least one output bypass path for providing a direct connection between an output from one of a plurality of LEs and at least one I/O block, where the at least one output bypass path does not travel through a multiplexer between the plurality of LEs and the at least one I/O block, as defined by applicant's amended independent claim 1. Nor does Agrawal show or suggest the corresponding feature in either of applicants' claims 27 or 30.

Schlecher, which was applied by the Examiner for the alleged teaching of specific elements of certain dependent claims, does not make up the deficiencies of Agrawal in failing to show or suggest the claimed invention.

For at least the foregoing reasons, applicants respectfully submit that amended independent claims 1, 27, and 30 are patentable. Accordingly, dependent claims 2, 4, 7-10, 12-26 are also patentable. Applicants respectfully request that the rejections of claims 1, 2, 4, 7-10, 12-27, and 30 be withdrawn.

Applicants' Reply to the Objection of Claims 3, 5, 6, and 11

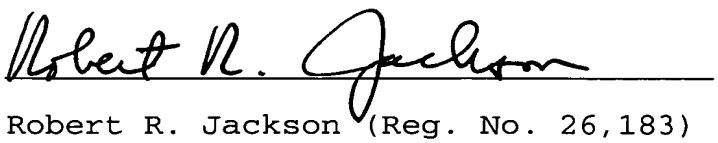
For at least the reasons set forth above, applicants respectfully submit that independent claim 1 is patentable. Accordingly, each of dependent claims 3, 5, 6, and 11 should also be patentable. Applicants respectfully request that the objection to claims 3, 5, 6, and 11 be withdrawn.

Conclusion

For at least the reasons set forth above, applicants respectfully submit that this application is in

condition for allowance. Reconsideration and prompt allowance of this application are respectfully requested.

Respectfully submitted,



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